## IN THE CLAIMS

1. (Currently amended) A method of manufacturing an MIM capacitor, which includes a lower electrode, a first wiring layer that is located below or in a same level with the lower electrode and is insulated from the lower electrode, and an upper electrode that overlaps with the lower electrode and contacts the first wiring layer through a contact hole in a [[the ]]dielectric layer that is between the upper electrode and the lower electrode, the method comprising:

forming the [[a ]]dielectric layer on the entire surface of a substrate on which the lower electrode and the first wiring layer are formed;

patterning the dielectric layer to form the [[a ]]contact hole through which the surface of the first wiring layer is exposed; and

forming the upper electrode comprising a material to contact the first wiring layer through the contact hole.

2. (Original) The method of claim 1, wherein patterning the dielectric layer comprises:

forming a dual hard mask (DHM) on the dielectric layer; and

etching the dielectric layer using the DHM as an etching mask.

3. (Currently amended) The method of claim 2, wherein forming the DHM on the dielectric layer comprises:

forming on the dielectric layer a DHM lower layer comprising [[of ]]the same ~~conductive~~ material that is used to form the upper electrode;

forming a DHM upper layer of a dielectric material on the DHM lower layer;

forming a photoresist pattern that defines the contact hole on the DHM upper layer;

etching the DHM upper and lower layers using the photoresist pattern as an etching mask; and

removing the photoresist pattern.

4. (Original) The method of claim 3, wherein the DHM upper layer and the dielectric layer are formed of the same material to the same thickness.

5. (Original) The method of claim 3, further comprising substantially etching away the DHM upper mask at the same time as etching the dielectric layer.

6. (Original) The method of claim 5, wherein forming the upper electrode comprises:

forming a conductive layer on the DHM lower mask and within contact hole; and

patterning the conductive layer and the DHM lower mask.

7. (Currently amended) The method of claim 2, wherein forming the DHM on the dielectric layer comprises:

forming a dielectric DHM lower layer on the dielectric layer, the DHM lower layer having an etch selectivity relative to ~~a higher etching rate than~~ the dielectric layer;

forming a dielectric DHM upper layer on the DHM lower layer;

forming a photoresist pattern that defines the contact hole on the DHM upper layer;

etching the DHM lower and upper layers using the photoresist pattern as an etching mask; and

removing the photoresist pattern.

8. (Original) The method of claim 7, wherein the DHM upper layer and the dielectric layer are formed of the same material to the same thickness.

9. (Original) The method of claim 7, wherein etching the dielectric layer using the DHM as an etching mask comprises:

substantially etching away the DHM upper mask at the same time as etching the dielectric layer; and

removing the DHM lower mask to expose a surface of the dielectric layer.

10. (Original) The method of claim 9, wherein forming the upper electrode comprises:

forming a conductive layer on the dielectric layer and within the contact hole; and

patterning the conductive layer to complete the upper electrode.

11. (Withdrawn) A method of forming an MIM capacitor, comprising:

forming a lower electrode and a first wiring layer on a substrate;

forming a dielectric layer on the resulting substrate;

patterning an etching mask that is disposed on the dielectric layer;

etching the dielectric layer through the etching mask to form a contact hole;

removing the etching mask;

forming an upper electrode that is disposed over the dielectric layer; and

forming a contact through the contact hole between the first wiring layer and an underside of the upper electrode.

12. (Withdrawn) The method of claim 11 wherein forming an upper electrode and forming a contact occur simultaneously.

13. (Withdrawn) The method of claim 11 wherein patterning an etching mask comprises:

forming a DHM layer; and

patterning the DHM layer.

14. (Withdrawn) The method of claim 13 wherein forming a DHM layer comprises:

forming a DHM lower layer; and

forming a DHM upper layer of the same material used to form the dielectric layer.

15. (Withdrawn) The method of claim 14 wherein forming a DHM upper layer comprises:

forming a DHM upper layer of the same material used to form the dielectric layer to a thickness approximately equal to that of the dielectric layer.

16. (Withdrawn) The method of claim 14 wherein forming a DHM lower layer comprises:

forming a DHM lower layer that is etch-selectable from the dielectric layer.

17. (Withdrawn) The method of claim 14 wherein forming a DHM lower layer comprises:

forming a DHM lower layer of a same material used to form the upper electrode.

18. (Withdrawn) A method of forming an MIM capacitor, comprising:

forming a lower electrode and a first wiring layer on a substrate;

forming a dielectric layer on the resulting substrate;

forming a DHM layer on the dielectric layer;

patterning the DHM layer;

etching the dielectric layer through the patterned DHM layer to form a contact hole;

removing at least one of the DHM layers;

forming an upper electrode that is disposed over the dielectric layer; and

forming a contact through the contact hole between the first wiring layer and an underside of the upper electrode.

19. (Withdrawn) The method of claim 18 wherein forming a DHM layer comprises:

forming a lower DHM layer; and

forming an upper DHM layer of a same material as used to form the dielectric layer.

20. (Withdrawn) The method of claim 19 wherein forming an upper DHM layer comprises forming an upper DHM layer of a same material as used to form the dielectric layer to a same thickness as the dielectric layer.

21. (Withdrawn) The method of claim 19 wherein forming a lower DHM layer comprises:

forming a layer that has a different etching rate than the dielectric layer.

22. (Withdrawn) The method of claim 19 wherein forming a lower DHM layer comprises:

forming a layer of a same material as used to form the upper electrode.